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Potential influence on copper electrodeposition on scratched silicon surfaces

Y. Zhang · E. Balaur · P. Schmuki

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Abstract Various methods can be used to pattern surfaces with small features. In the present work, a micro-indenter was used to scratch the Si surface to create sub-micrometer structures. The influence of the electrochemical potential on copper nucleation, growth and morphology was studied on this scratched silicon surface. Copper deposition either in the opening of an insulating oxide layers made by scratching with an indenter tip or in oxide free Si surface was observed with Scanning Electron Microscopy (SEM). The nucleation and growth morphology of copper at high voltage pulse on both oxide covered and oxide free silicon surfaces were also studied. We demonstrate that thin oxide layers can act as a very efficient resist even at comparably high voltages.

Keywords Electrochemical metal deposition · Scratching · Silicon · Copper

Introduction

The ability to generate small structures is central to modern science and technology. Selective metal deposition on semiconductor surfaces has been realized as an interest topic due to possible applications in microelectronics, especially in the formation of micro- and nano-structures on semiconductors.

Patterned metal deposition on semiconductor surfaces is typically carried out by different indirect ways such as photolithography combined with metal evaporation, electrodeposition or molecular beam epitaxy (MBE). The limiting factor in traditional photolithography is the wavelength of the UV lamps. To increase the local resolution several approaches were used such as eletron-beam lithography [1, 2]. Atomic force microscopy (AFM) sensitisation of an organic layer [3, 4] or a direct modification of the silicon substrate by local depassivation by scanning an AFM tip under bias [5] has been investigated. All these techniques are based on a local activation of the Si surface either by mask removing or by direct activation.

For example for a selective activation, it has been demonstrated that porous Si growth can electrochemically be initiated preferentially at surface defects created in an *n*-type Si substrate by Si^{++} focussed ion beam (FIB) bombardment [6]. On the other hand it was shown that FIB defect creation in *p*-type Si enables a selective metal electrodeposition in the defective regions [7]. In these cases, introduction of active defects on the semiconductor surface allows to realize patterning in the sub-micrometer range. We investigated the possibility to selectively electrodeposit metals into mechanically generated surface defects on semiconductors, e.g. scratching with a micro-indenter or an atomic force microscope tips. Selective electrochemical copper deposition was obtained on AFM patterned nanoscratches. The AFM scratches were produced on either the native oxide layer 10 nm oxide covered silicon surfaces [8, 9]. Recently organic monolayers were used as an resist for copper immersion plating on Si [10].

The deposition of metals onto semiconductor surfaces is influenced by several factors. The interaction energy between many semiconductors and metals is relatively weak so that the deposition of metals onto semiconductor surfaces is not always straightforward. The electrodeposition of copper on silicon follows typically a 3D island growth (Volmer-Weber) mechanism due to the weak interaction energy. Therefore the applied voltage is expected to have a significant effect on the deposition behaviour.

Y. Zhang · E. Balaur · P. Schmuki (✉)
Dept. Materials Science, WW4-LKO, University of Erlangen–Nuremberg, Martensstr. 7, D-91058 Erlangen, Germany
e-mail: schmuki@ww.uni-erlangen.de

In order to achieve optimised metal patterns a detailed understanding of the mechanism and morphology of the nucleation [11–14], growth and the role of parameters such as applied potential and electrolyte composition [12, 14–16] is required. Several authors have investigated the growth of electrodeposited metals with emphasis on regimes characterized by fractal geometry [17], dendrite growth [18] and the investigation of copper electrodeposits in a spherical geometry [19].

This work extends our previous studies in various ways. Particularly the potential influence was studied to explore the limits of selective copper electrodeposition in the scratched regions of the surface. The different surface morphology was observed with SEM.

Experimental

Experiments were performed on 4 different types of substrates: *p*-Si (100) and *n*-Si (100) covered with 10 nm oxide layer, *p*-Si (100) and *n*-Si (100) covered with the native oxide layer. Resistivity of oxide free Si wafer is approximately 1–10 $\Omega\cdot$ cm (Wafer World Inc., Florida). Cleaved silicon pieces of 15 $\times$ 15 mm surfaces were sonicated in acetone, isopropanol and methanol and then dried in a nitrogen stream. The chemicals used were acetone, isopropanol, methanol, $CuSO_4{\cdot}5H_2O$ analysis grade (Merck, Germany), and H_2SO_4 (suprapure grade, Merck, Germany). In order to produce scratches through the oxide layer, a micro-indenter (Leitz miniload indenter, Germany) with a four-sided diamond tip was used. A normal load of 49 mN was applied for all experiments and the scratches were made by a displacement of the sample stage, which was an *x*-*y* table. The scratches were around 20 nm deep and approximately 2 μm wide.

Before metal deposition, the scratched Si pieces were sonicated in pure water for 5 min to remove debris formed during the scratching. Subsequently the samples were dipped in a Teflon beaker containing 1% HF solution for only 30 seconds to remove oxide that may have been reformed in the grooves after scratching, but keep the rest of surface still covered with thermal oxides.

Electrodeposition was carried out by cathodic potential step in different $CuSO_4$ and H_2SO_4 solutions at room temperature and in a dark box to avoid any uncontrolled photocurrent. Electrical contact to the Si pieces was established by smearing InGa eutectic (99.99%) on the backside of the sample. The sample front side was pressed against an O-ring of a polymer-cell leaving 0.126 cm^2 exposed to the electrolyte. The electrochemical cell consisted of a standard three-electrode configuration. Platinum gauze served as a counter electrode and a silver/silver chloride (Ag/AgCl, $E = 236$ mV vs. SHE electrode) was used as a reference electrode. The experiments were carried out with a Jaissle 1030 DA potentiostat connected to a data acquisition system. For higher voltage steps a special "high voltage" potentiostat (Jaissle IMP 88 PC-200V) was used.

Scanning electron microscope (SEM) images were acquired with a SEM-JEOL 6400 equipped with a tungsten filament.

Results and discussion

In order to assess key factors for scratch filling a variety of experimental parameters were screened on oxide-covered samples. For these experiments the different Si samples were scratched with a micro-indenter producing an *L*-shaped (top view) V-groove (side view) in the surface. The electrolyte concentration was varied with either 0.1 M $CuSO_4$ and 0.5 M H_2SO_4 or 0.01 M $CuSO_4$ and 0.5 M H_2SO_4.

Experiments showed that applied potential has a significant influence on the morphology of the deposit. Figure 1 shows changes in the morphology of the copper deposits under different voltages. The deposition was carried out for 5 s on *n*-type Si covered with 10 nm oxide layer carrying the *L*-shape scratch at different potentials (vs Ag/AgCl): (a) -1 V, (b) -2 V, (c) -5 V. Copper with a concentration of 0.01 M $CuSO_4$ and 0.5 M H_2SO_4 electrolyte was selected because

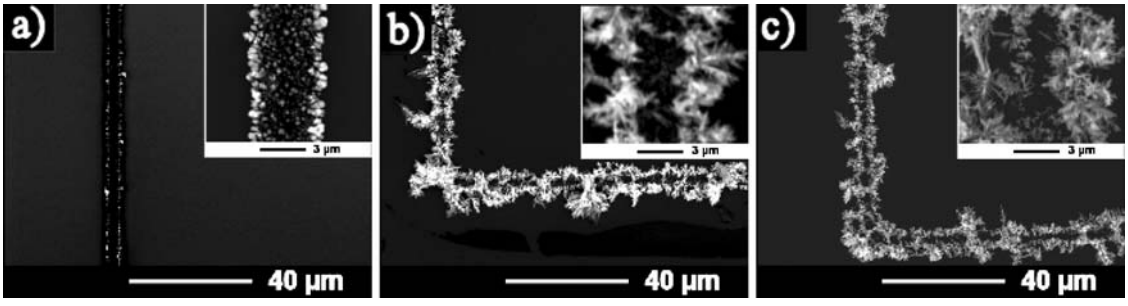

Fig. 1 SEM images of copper deposited on scratched *n*-Si(100) covered with 10 nm oxide. The scratch was performed with a micro-indenter ($F = 49.03$ mN) through the oxide. The deposition was carried out in $CuSO_4$ (0.01 M) + H_2SO_4 (0.5 M) electrolyte for 5 s under different cathodic voltage. (a) -1 V, (b) -2 V, and (c) -5 V vs. Ag/AgCl

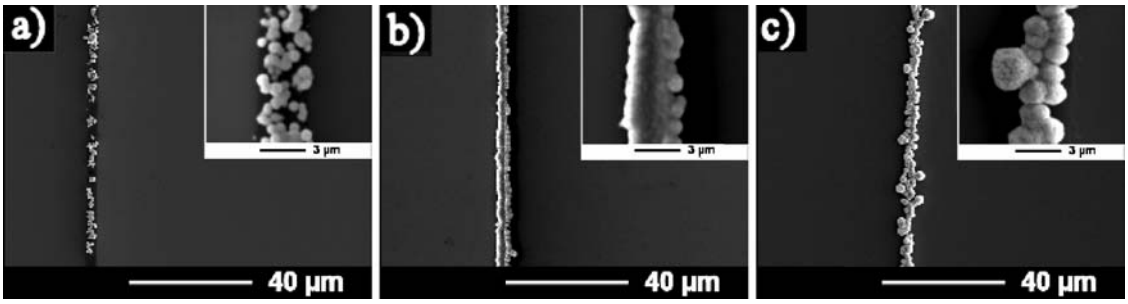

Fig. 2 SEM images of copper deposited on scratched *p*-Si (100) covered with 10 nm oxide. The scratch was performed with a micro-indenter ($F = 49.03$ mN) through the oxide. The deposition was carried out in $CuSO_4$ (0.1 M) + H_2SO_4 (0.5 M) electrolyte for 10 s under different cathodic voltage. (a) −1 V, (b) −5 V, and (c) −10 V vs. Ag/AgCl

at higher overvoltage the copper deposited from higher concentration electrolytes showed very bad adhesion on *n*-type Si. It can be seen clearly from the SEM images that copper preferentially deposits into the scratches at all voltages. However the detailed morphology strongly depends on the applied voltage. At low voltages a granular structure of the deposits is obtained (Fig. 1(a)). And at relatively high voltages it yields dendrite morphology on *n*-type silicon. This effect starts over certain voltages e.g. –2 V, (Fig. 1(b)). Here, there are well-defined "backbones" with side branches. Keeping the same deposition time, but increasing the applied cathodic voltage, more copper is deposited in the scratched area but still in the shape of dendrite morphology (Fig. 1(c)). Figure 2 shows the copper deposited into the scratches on *p*-Si (100) covered with 10 nm oxide. The deposition was carried out in electrolyte (0.1 M $CuSO_4$ + 0.5 M H_2SO_4) for 10 s under different cathodic voltage: (a) −1 V, (b) −5 V, (c) −10 V. For *p*-type silicon, copper deposition under certain potential range shows different deposition behaviour and morphology compared with *n*-type silicon. In contrast to *n*-type Si, even at relative high voltage the deposits still have a globular morphology. These resemble micrographs of the structure of copper deposits in a spherical geometry [19]. On *p*-type Si surface the copper clusters grow slowly, even with longer deposition time, the overgrowth will not take place.

A key difference in the behaviours of *n*-type and *p*-type silicon surfaces can be ascribed to the electronic properties of the semiconductor. Under cathodic potential, *n*-type Si is in a current passing state, and electrochemical reactions are limited by activation control, while *p*-type Si is in a current blocking state, therefore reactions are limited by electrons overcoming the Schottky barrier. The cathodic deposition is hindered. Therefore at the same cathodic potential *n*-type silicon shows higher hydrogen evolution rate than *p*-type silicon. At relatively high cathodic voltages e.g. −5 V vs. Ag/AgCl, hydrogen evolution takes place both on top of copper and on Si substrate as well. High hydrogen evolution rate was found to be the detrimental for the adhesion of copper, since hydrogen bubbling can trigger a popping off of the deposits from the surface.

One could assume that once a Cu nucleus is formed on the Si surface, at moderate potential a globular growth takes place. Increasing the overvoltage, the nuclei size will be decreased and more nucleation sites will be generated. The deposition takes place in a very fast rate. In the following experiments very high cathodic voltages were used in this work to clearly identify the effect of the voltage on morphology of the copper deposit. Figure 3 shows the SEM images of copper deposition on 10nm oxide covered silicon surfaces carrying the *L*-shaped scratch. These experiments were carried out by a cathodic potential step of −100 V (vs. Ag/AgCl) in electrolyte (0.1 M $CuSO_4$ + 0.5 M H_2SO_4) with different time: (a), (d) 1 ms, (b), (e) 10 ms, (c), (f) 100 ms. Figure 3(a)–(c) show copper deposition on *p*-Si and (d–f) on *n*-Si respectively. At this high voltage, the growth is extremely fast. Clearly, from Fig. 3 it can be seen that in cases of copper deposited on both *p*-type Si and *n*-type Si, the nuclei are smaller than those deposited under lower overvoltage. Copper deposition on *n*-type silicon at −100 V for 10 ms in the high copper concentration electrolyte shows very good filling ability leading to homogenous and continuous line as can be seen from Fig. 3(e). In case of very high voltage (−100 V), there are a lot of nucleation sites and nuclei is very small. For a short time pulse, the copper will be deposited on the surface homogeneously. However after a longer deposition time an irregular structure of the copper deposit is observed (in Fig. 3(f)). Long deposition time leads to massive copper deposition combined with hydrogen evolution that again affects the adhesion. Nevertheless after "popping off" (in Fig. 3(f)), some copper remains and deposition continues at these locations forming irregular structures. Additionally it can be seen clearly from Fig. 3(f), that after longer deposition time at −100 V "break down" of the blocking silicon dioxide takes place, copper nuclei start being randomly deposited on the whole surfaces. This breakdown may be ascribed to either direct dielectric break down or H^+ inward migration through the SiO_2 layer followed by reaction to H_2 at the Si/SiO_2 interface, leading to internal H_2 gas formation and disbonding of the SiO_2 layer. Homogeneous copper filling was obtained under high voltage short time pulse

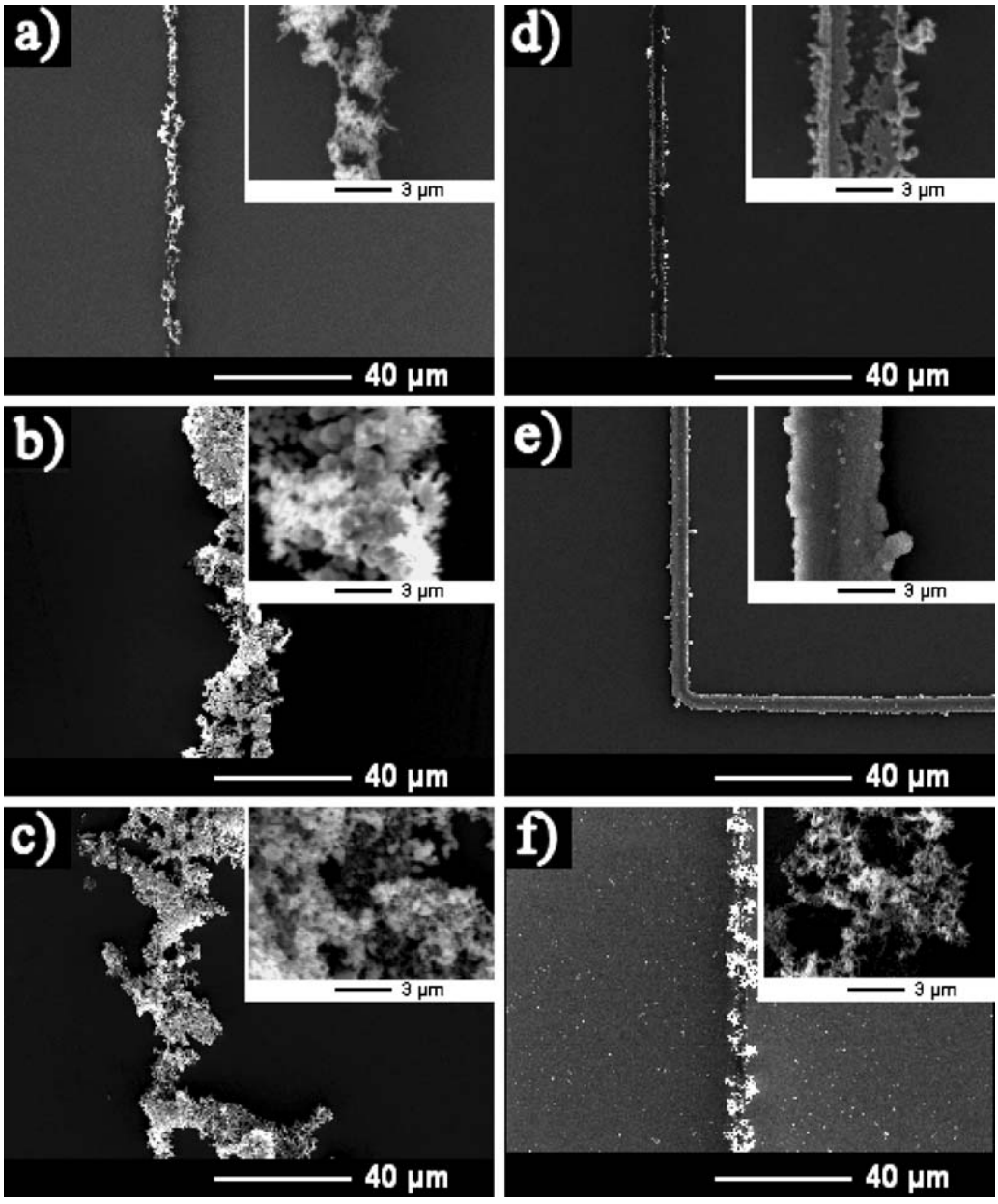

Fig. 3 SEM images of Cu deposited on scratched Si (100) covered with 10 nm Oxide, *p*-Si (a–c) and *n*-Si (d–f). The scratch was performed with a micro-indenter ($F = 49.03$ mN) through the oxide. The Cu deposition was carried out by a cathodic potential step of −100 V (vs Ag/AgCl) in $CuSO_4$ (0.1 M) + H_2SO_4 (0.5 M) electrolyte. (a), (d) 1 ms; (b), (e) 10 ms; (c), (f) 100 ms

for *n*-Si covered with 10 nm oxide layers. It is interesting that *p*-Si, which normally does not show overgrowth at relative high voltage (−10 V) compared with *n*-Si, shows a bigger overgrowth under the same condition at −100 V. This maybe due to the fact that copper and *p*-Si form a blocking metal-semiconductor junction at low cathodic voltages and this limits the overgrowth. It seems likely at −100 V metal-semiconductor junction may suffer from breakdown and therefore this self-limiting effect is lost and copper deposit grows rapidly (and like irregular microcrystals).

In order to see the effect of copper deposition on the scratched Si surface without oxide layer, we also investigated the oxide free silicon samples. For this, before electrodeposition the native oxide covered silicon samples were dipped into 1% HF for 1 min to remove the oxide layer. Figure 4 shows the SEM images after copper deposition. The experiments were carried out by a cathodic potential step to −100 V (vs. Ag/AgCl) in (0.1 M $CuSO_4$ + 0.5 M H_2SO_4) for different time: (a), c) 1 ms, (b) (d) 100 ms. In Fig. 4(a) and (b) copper was deposited on *p*-Si and (c,d) *n*-Si respectively. As we can

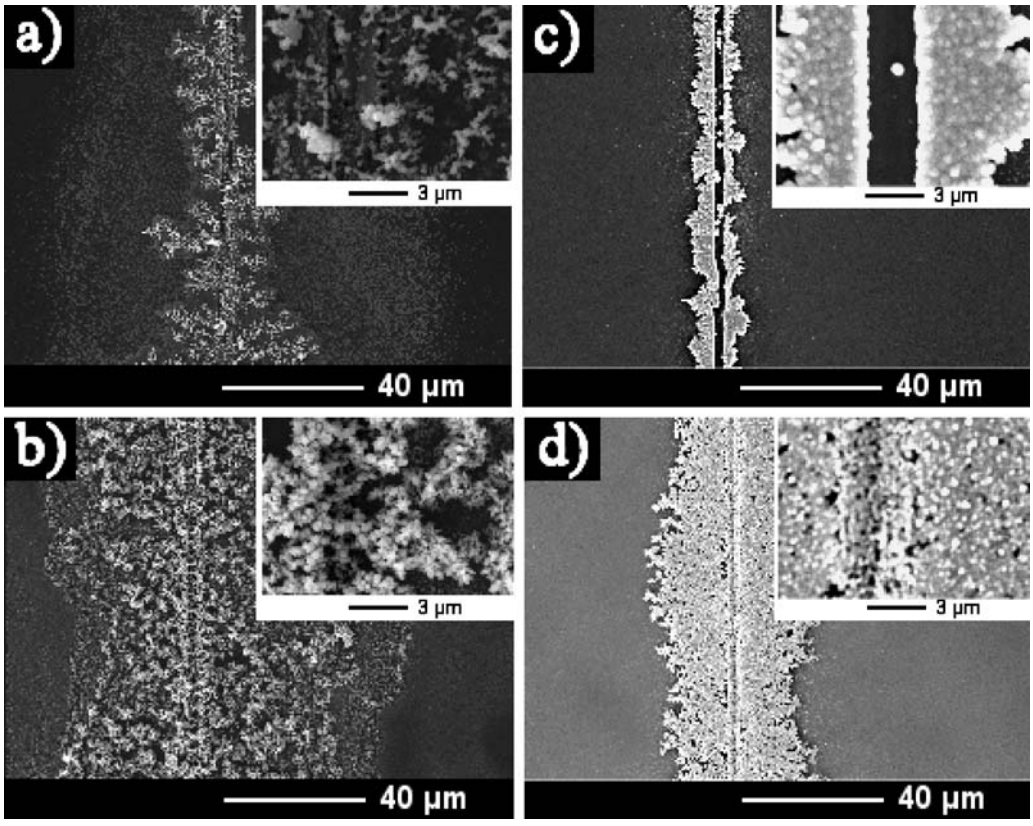

Fig. 4 SEM images of Cu deposited on scratched Si (100) *p*-Si (a, b) and *n*-Si (c, d). The scratch was performed with a micro-indenter ($F = 49.03$ mN) through the native oxide. The Cu deposition was carried out by a cathodic potential step of -100 V (vs Ag/AgCl) in $CuSO_4$ (0.1 M) + H_2SO_4 (0.5 M) electrolyte after dip into 1% HF for 1 min. (a), (c) 1 ms; (b), (d) 100 ms

see, copper is preferentially deposited in the scratched areas and the vicinities. It appears that copper nucleation starts on surface defects created during the scratching and on the plastic deformation zone. For sufficient short time pulses, copper can be selectively deposited near the surface defects but also into the scratches. This finding offers very promising possibilities for a direct structuring of Si surfaces. The copper deposits on *p*-type Si are ramified structures during the entire growth period. At high over voltage the deposition rate is very high, Cu^{2+} reduction takes place in a short time, which leads to irregular growth morphology. While on *n*-type Si, copper is first deposited on the edges of the scratch in a short time because there is high field on the edge as well. With longer deposition time, the copper deposits appear to be a roughly fractal film with open cells. The adhesion of such film becomes much worse than the single copper nuclei.

Conclusion

In this paper we studied the nucleation and growth morphology of copper deposit on the scratched oxide free silicon and Si/SiO_2 surfaces. Effects of the applied potential on copper deposition on different type of silicon wafers were obtained. Different voltage leads to different copper growth morphologies. For *n*-type Si, at potential over -1 V the morphology changes from granular to a dendrite structure. However, *p*-type Si kept spherical geometry up to relatively high voltage. At very high voltages and a short pulse the copper deposition takes place with a high rate and in this situation both *n*-type and *p*-type Si show an irregular morphology of copper deposits. Hydrogen evolution is responsible for poor adhesion of the copper deposits and its irregular morphology. Under high voltages and short pulse, copper was preferentially deposited into scratched locations on oxide free *n*-type and *p*-type Si.

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